

# Power Optimization using Low-Transition Rate based LFSR Pattern Generator

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**Abstract**-Dynamic power dissipation has been increased exponentially with the excessive switching of nodes inside the digital electronic circuits. Power dissipation on these circuits are highly input pattern dependent. This work exploits the generation of efficient input patterns with the ability to reduce maximum switching activity in the circuit by using linear feedback shift register (LFSR) technique. This approach is further modified by the insertion of the low-transition density with highly correlated signals in the LFSR-based patterns. The transition between different patterns reduces the substantial amount of switching activity in the circuit. Reduction in transition results the low dynamic power consumption. Power consumption have been estimated by using standard ISCAS 85 and 89 benchmark circuits. The experimental results demonstrate that power can be significantly optimized using this approach.

**Keywords**-Switching Activity, Digital Patterns Generator, Power Optimization, Benchmark Circuits

## I. INTRODUCTION

Power analysis of electronic circuit design is a major challenging task due to the accurately analyzing power without the direct information of the design details. With the wide utilization of portable systems, low-power chip design is becoming an increasingly important focus of modern research. Therefore, a suitable power optimization (reduction) approach is very much important in both testing mode and functional to design high-performance circuits, so that reliability and satisfactory performance can be efficiently achieved. In power estimation methods, input patterns play a significant role. Low -power dissipation can be achieved only by focusing on input stream. Digital patterns can be generated from pattern generator such as linear feedback shift register (LFSR), for which different parameters can be observed to produce maximum power reduction without affecting the performance of the circuit. Input pattern generator can be carefully designed to meet all requirements for power reduction.

Several researchers have been proposed to optimize power by reducing the toggle rate of input

patterns. A well-known technique was introduced in [i], [ii] to select the LFSR seed for energy reduction. It was analyzed the impact of LFSR's polynomial and seed selection on the core-under-test switching activity. Another approach was proposed for the design of low-transition test pattern generator [iii]. Two LFSRs with different number of registers have been used to control inputs with high transition densities. Based on cellular automata, a low-power pattern generator was proposed in [iv] to reduce the testing power of the circuit-under-test. In [v] the authors used clock gating technique in which odd and even vectors in the scan chain has been controlled by two non-overlapping clocks reducing power by factor of two. Single-input change sequence was generated in [vi] by using ring generator which can effectively reduce the test power. In [vii], the efficient selection of the most suitable subset of scan cells for gating along with their gating values were studied. The authors in [viii], reduced the number of input patterns to obtain the target fault coverage to minimize the testing power. The non-detecting patterns have been filter out by using gate-based logics, however, the experimental result produces with high delay. The power reduction is achieved by increasing the correlation between consecutive test patterns by reducing the switching activity in [ix]. Furthermore, the insertion of intermediate patterns was used by combining two pattern generation schemes in LFSR-based patterns. The LFSR was modified for low-energy consumption by adding weights to tune the pseudo random vectors for different probabilities.

Previously we proposed an accurate power macro-modeling techniques in [x], [xi], [xii], [xiii] that implemented on IP-based digital test systems. In this work, we further continue this research and developed efficient pattern generator for low-power dissipation in electronic circuits. This paper exploits the generation of input patterns with the ability to reduce maximum transition activity in the digital circuits by using LFSR technique. Our approach proposed the insertion technique of low-transition density with high correlated signals in the LFSR-based patterns. Power consumption have been estimated by using standard ISCAS 85 and 89 benchmark circuits. The experimental results demonstrate that power can be significantly optimized using this approach.

The paper is organized as follows. The traditional linear feedback shift register and proposed low-transition rate based LFSR pattern generator is discussed in Section II, and III respectively. In Section IV, the experimental results and discussion is given. The Section V summarizes the work.

## II. LINEAR FEEDBACK SHIFT REGISTER

A conventional architecture of linear-feedback shift register is used as a pattern generation. It is a shift register whose input bit is driven by XOR gate and it is a linear function of its previous state as shown in figure 1. When LFSR receives clock signals, it advances the signal within the register from one bit to the next most-significant bit. Some outputs of the register are used in XOR configuration to make a feedback input to the registers.

The shift register length is determined by the highest polynomial degree. The locations of the feedback taps of the register corresponds the exponents in the polynomial. The bit values at different taps are added by XOR operation or by modulus 2. The result is a feedback to the input of the register. On every clock signal a new bit appears at the input of the register, while in every flip-flop a bit generates to the next flip-flop.

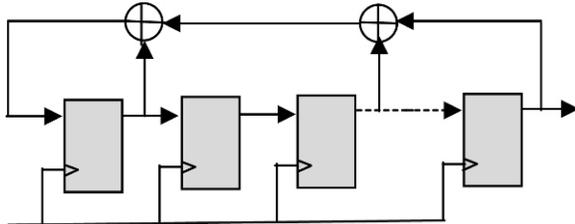


Fig. 1. Conventional Linear feedback shift register

## III. LFSR PATTERN GENERATOR

In this section, we propose a low-transition rate based modified LFSR technique. This approach elaborates the digital pattern generation scheme by using LFSR into low-transition patterns making them applicable for low-power applications without affecting performance of the circuits. The technique applied on generated patterns with low-transition density between selected pairs of the pattern. Generated pattern stream is then applied to the input of ISCAS 85 and 89 benchmarks of combinational and sequential circuits.

The low-transition rate LFSR pattern generator has  $n$  number of flip-flops ( $A_0, A_1, \dots, A_{n-1}$ ) with each time step  $A_i$  takes the value of  $A_{i-1}$  for  $i > 1$ .  $A_0$  updates the value to the feedback function  $f: \{0,1\}^n \rightarrow \{0,1\}$  and  $A_{n-1}$  is the output of the LFSR as shown in Fig. 2. A sequence  $(x_i)_{i \in \mathbb{N}}$  is generated by a shift register satisfying

the  $n$ -term recursion  $x_{i+n} = f(x_i, \dots, x_{i+n-1})$ .

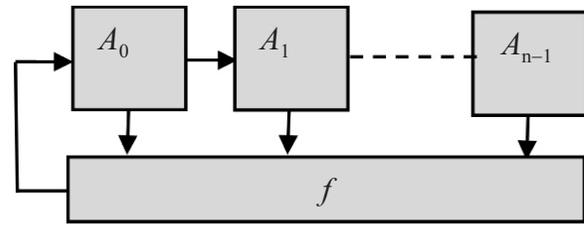


Fig. 2. Feedback shift register

### A. Word-wise sequence generation

LFSR is used as a pattern generator consists of several of D Flip-flops, XOR gates in the feedback path and is initialized with a seed value as shown in Fig. 2. Number of bits in the pattern is given by the polynomial which is equal to the number of primary inputs of a combinational or sequential circuit. Patterns are generated by LFSR by using pseudo random in nature with high toggle rate and high transition density. If  $n$  is the maximum length of LFSR then it produces an  $n$ -sequences, since the XOR of zeros will remain zero and state cannot be changed.

The transition rate LFSR pattern generator used an array of words  $(b_0, b_1, \dots, b_n)$  indicates the internal state of the register. The shift operation is implemented by calling the rotation instructions and shift of the value as shown in Fig. 3.

```

Pattern generator sequence of input
pattern ()
    num_gen = 0;
    Generation of randomly signals;
Rshift bn-1;    -- right-shift by 1
for m= n-1 to n-1 do
    rcrbk;      -- right roll by 1 with
the use of carry-flag
end for;
    
```

Fig. 3. Flow of the pattern generator

In case of polynomial of feedback has non-zero coefficients, then the feedback value can be determined by  $f_b = a(f_{b0}) + a(f_{b1}) + \dots + a(f_{bk})$ . There are several non-zeros coefficients of the feedback polynomial stored in  $f_b$ . We compute coefficient  $a$  and feedback  $f_b$ , then count the non-zero bits in  $a$  and  $f_b$  modulo 2.

Let  $w$  is the word size and we assumed  $w = 2^n$ . The length  $l$  of LFSR is divisible by  $w$  and  $l = w\hat{l}$ . The LFSR may be defines a linear mapping procedure from its initial state  $(x_0, x_1, \dots, x_{n-1})$  to output sequence  $(x_i)_{i \in \mathbb{N}}$  in (1):

$$V: (x_0, x_1, \dots, x_{n-1}) \rightarrow (x_0, x_1, \dots, x_{i-1}) \quad (1)$$

The pattern generator parity check matrix can be expressed in (2):

$$B = \begin{bmatrix} v_0 & \cdots & v_{n-1} & -1 & 0 & \cdots & 0 \\ \vdots & \ddots & & \vdots & & & \\ 0 & \cdots & 0 & v_0 & \cdots & v_{n-1} & -1 \end{bmatrix} \quad (2)$$

According to the coding theory based on LFSR sequences [xiv], the code  $V$  can have generator matrix in (3):

$$I = \begin{pmatrix} 1 & 0 & v_{n,0} & \cdots & v_{N-1,0} \\ \cdots & & & & \\ 0 & 1 & v_{n,n-1} & \cdots & v_{N-1,n-1} \end{pmatrix} \quad (3)$$

We have  $(x_0, x_1, \dots, x_{N-1}) (x_0, x_1, \dots, x_{n-1}) I$ , i.e.

$$x_c = \sum_{i=0}^{n-1} v_{c,i} x_i \quad (4)$$

The linear representation of the related component  $x_c$  in (4) is related to the initial state.

The arrangement of taps for feedback in LFSR can be expressed in arithmetic as a polynomial mod 2. This means the coefficients of the polynomial must be either 1 or 0. In Fig. 2, the feedback polynomial  $x^{16} + x^{14} + x^{13} + x^{11} + 1$  is taken. In case of primitive polynomial of low-transition rate LFSR has becomes a maximal length. Following conditions are necessary to meet the criteria of feedback polynomial:

- The number of taps should be even.
- The set of taps, taken all together, not pairwise (i.e. as pairs of elements) must be relatively prime. In other words, there must be no divisor other than 1 and common to all taps.

LFSRs can never have the zero value, since every shift of a zeroed LFSR remain as zero. The low-transition rate LFSR must be initialized, i.e., seeded, to a non-zero value. When the LFSR holds 1 and is shifted once, its value always be the value of the polynomial mask. When the register contains all zeros except the most significant bit, then the next several shifts gives the high-bit shift to the low-bit with zero fill. For example, any 8-bit shift register with a primitive polynomial can eventually generate the sequence 0x80, 0x40, 0x20, 0x10, 8, 4, 2, 1 and then the polynomial mask.

#### B. Insertion of low-transition density pattern

In this approach, we introduce a switching mechanism to insert low-transition density signals in the LFSR-based patterns. The Fig. 4 demonstrates this mechanism. Any two consecutive patterns of LFSR are compared with each other to reduces the number of switching activity in the patterns. At any bit location, when transition occurs between two input signals, a pattern generator insert either 0 or 1 (random bit) at the specific position. While for remaining locations, bits remain same as of the previous pattern. In the Fig, the selection of random bit  $b$  is made on the base of transition density (TD). Patterns generated with random bit 1 and random bit 0 are stored in the memory.

The selection of pattern is decided by evaluating the value of TD for each newly generated intermediate pattern. A pattern with low-transition density is sent to output and gives new patterns between original pattern pairs. The new pattern is generated from the insertion of random bit at a place of transitions so it eliminates the consecutive switching. Due to this signal insertion mechanism, the improved correlated patterns are generated for the circuit. Mathematically, this mechanism can be expressed in the following example.

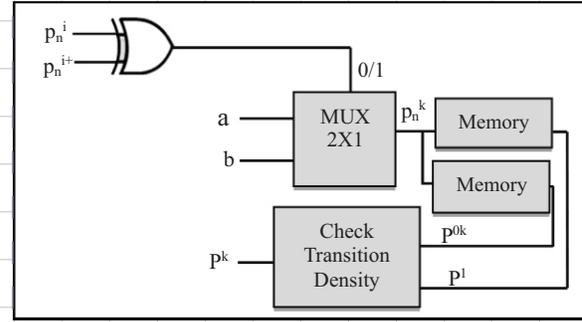


Fig. 4. Schematic diagram for first modification

Assume we have two patterns generated by LFSR as:

$$p^i = (p_0^i, p_1^i, \dots, p_{n-1}^i, p_n^i) \quad (5)$$

$$p^{i+1} = (p_0^{i+1}, p_1^{i+1}, \dots, p_{n-1}^{i+1}, p_n^{i+1}) \quad (6)$$

where  $n$  represents the number of bits in the input pattern, which is equal to the number of primary inputs of the circuit. All bits are compared with each other from both patterns taking one bit at a time (see Fig 4).  $b$  is the random bit which takes value of 0 and 1 in generating  $P^{0k}$  and  $P^{1k}$  patterns respectively. Transition densities for both new patterns are calculated. Pattern with low-transition density gives output pattern  $P^k$  as given in (7) and (8):

$$\text{for } p_j^i \oplus p_j^{i+1} = 0, \quad p_j^k = p_j^i \quad (7)$$

$$\text{for } p_j^i \oplus p_j^{i+1} = 1, \quad p_j^k = b \quad (8)$$

Where  $1 \leq j \leq n$ ,  $1 \leq i \leq 2^n$  in (11) and (12):

$$P^{0k} = (p_0^{0k}, p_1^{0k}, \dots, p_{n-1}^{0k}, p_n^{0k}) \text{ with } b = 0 \quad (9)$$

$$P^{1k} = (p_0^{1k}, p_1^{1k}, \dots, p_{n-1}^{1k}, p_n^{1k}) \text{ with } b = 1 \quad (10)$$

If  $TD(P^{0k}) < TD(P^{1k})$  in (11):

$$P^k = P^{0k} \text{ else } P^k = P^{1k} \quad (11)$$

where TD is the transition density and it is the ratio of transitions to the number of unit intervals in a serial data stream. For unit interval  $T$  with  $N(t)$  number of transitions, we have transition density as  $TD = N(t)/T$ .

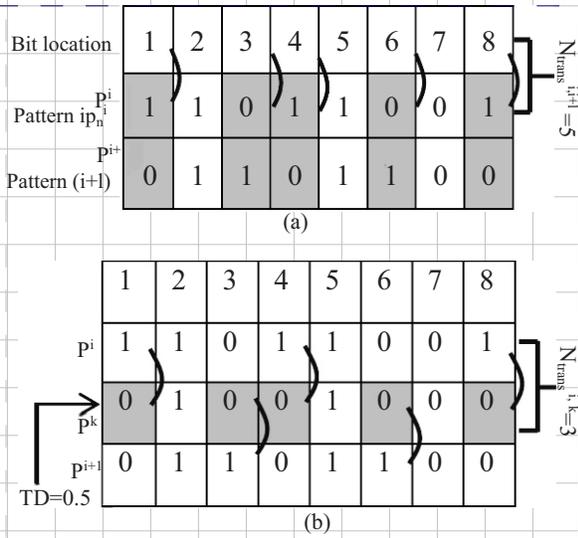


Fig. 5. Example of low-transition densities (a) Placement of bits (b) with 0.5 transition density

In case of switching activity occurs, the XOR output produces 1 and the random bit is inserted at this specific location. When both patterns are generated i.e. pattern with random bit 1 and random bit 0, the transition density is calculated and low-transition density pattern is send to the output. In case of no switching activity occurs, the XOR of the two selected bits give us 0 values. Hence, the newly generated bit remains same as of the previous bit.

#### IV. EXPERIMENTAL RESULTS

Previously, we have proposed power estimation techniques for system-on-chip (SoC) based systems in [x], [xi], [xii], [xiii]. In this section, the experimental work in evaluated on ISCAS 85 and 89 benchmark circuits. In experiments, power analysis is obtained for these benchmarks circuits. The power is analyzed for these patterns i.e. patterns generated by conventional LFSR and the patterns generated by low-transition pattern generator. Furthermore, the fault coverage is calculated by using parallel fault simulation method. The following summarized steps are used in the power analysis and fault coverage.

1. First patterns are generated using LFSR on Matlab.
2. ISCAS 85 and 89 benchmarks are implemented on Xilinx software using random input patterns generated in step 1.
3. The switching activity is recorded from VCD file in Xilinx. Power is analyzed on Xpower analyzer through generated VCD file.
4. Fault coverage is calculated on Xilinx and faults are inserted in benchmark circuits and parallel fault simulation method is used for detecting the faults.
5. The modified low-transition patterns are

generated using same seed as used for general LFSR using Matlab tool.

6. Step 2 and 3 are repeated to get power and fault coverage results for modified patterns.
7. Power is analyzed for ISCAS 85 and 89 benchmark circuits as well as fault coverage is obtained using fsm fault simulator.

The dynamic power is compared with general LFSR and modified LFSR based pattern generators using (12):

$$P_{dyn} = \frac{P_{dyn\_LFSR\_gen} - P_{dyn\_LFSR\_mod}}{P_{dyn\_LFSR\_gen}} \times 100 \quad (12)$$

The fault coverage for ISCAS benchmark circuits are estimated using (13):

$$Fault\ Coverage = \frac{Detected\ Faults}{Total\ Faults} \times 100$$

Table 1 demonstrate the results of power comparison between general LFSR and modified low-transition rate LFSR based pattern generators. The list

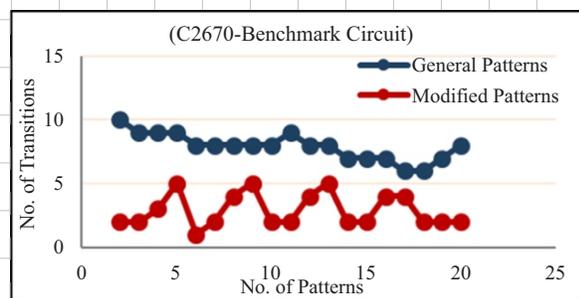
TABLE I  
POWER ANALYSIS RESULTS FOR ISCAS 85/89 BENCHMARKS

Sr. #	Circuit	General LFSR	Modified LFSR	%age Power reduction $\Delta P_{dyn}$
		Dy. Power (mW)	Dy. Power (mW)	
1	C17	0.023	0.014	39.131
2	C432	0.130	0.060	53.842
3	C499	0.210	0.125	40.470
4	C880	0.322	0.214	33.540
5	C1908	0.619	0.419	32.311
6	C2670	0.788	0.612	22.332
7	C3540	0.899	0.521	42.043
8	S27	0.013	0.009	30.762
9	S208	0.110	0.089	19.094
10	S298	0.210	0.116	44.764
11	S344	0.343	0.239	30.320
12	S349	0.398	0.220	44.721
13	S382	0.432	0.310	28.241
Average		0.346	0.227	35.503

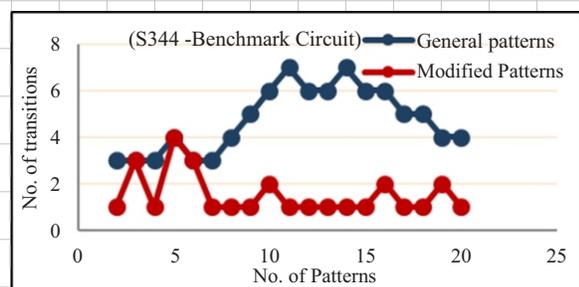
of the ISCAS 85 and 89 benchmark circuits are shown in the second column of Table I. The ISCAS-85 benchmark represents the combinational circuits and ISCAS-89 are the sequential circuits. The dynamic power dissipation of both generators are shown in third and fourth columns. The average power consumed by the general and modified LFSR based pattern generators are 0.346mW and 0.227mW respectively. The percentage of dynamic power reduction is

shown in fifth column of the Table. It is evident from Table I, that the results of our modified pattern generator reduce the average dynamic power till 35.50%. A substantial power reduction has been achieved by using our approach.

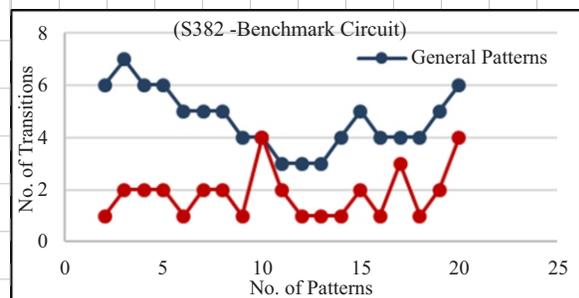
Patterns generator is also utilized for the fault coverage analysis in both digital combinational and sequential benchmark circuits. The results demonstrate that both general and modified LFSRs give 99% fault coverage. However, patterns used for detecting faults are less for modified LFSR pattern generator. The error range varies from (-3.1-+2.8) between both generators.



(a)



(b)



(c)

Fig. 6. Comparison of general patterns and modified low-transition patterns of ISCAS benchmarks (a) C2670 (b) S344 (c) S383

Low-power pattern stream significantly reduces the number of transitions among different patterns. Figure 6 (a),(b),(c) demonstrates the number of transitions occurs by using both pattern generators of different combinational and sequential benchmark circuits. Sample of 20 patterns are randomly chosen

and transitions are calculated by taking pair-wise patterns. The general patterns generator has large number of transitions. While by inserting the intermediate patterns, transition between two different patterns reduces the substantial amount of switching activity in the circuit. Reduction in transition results the low dynamic power consumption.

## V. CONCLUSION

This paper presents the generation of input patterns with the ability to reduce maximum switching activity in the circuit by using linear feedback shift register technique. This approach is modified by the insertion of the low-transition density with high correlated signals in the LFSR-based patterns. Furthermore, dynamic power is analyzed with our inserted low-transition density based LFSR technique. Power consumption and fault coverage have been estimated by using standard ISCAS 85 and 89 benchmark circuits. The experimental results demonstrate that power and fault coverage can be significantly optimized using this approach. Currently, we are implementing this approach on more complex circuits.

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