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An Improved PWM Technique to Reduce Total Harmonic Distortion of Multilevel Inverters

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Abstract- Regardless of its progressive popularity, the presence of unwanted harmonics in the voltage output of multilevel inverters is a critical concern. These harmonics indicate dreadful results for electrical as well as mechanical equipment: (1) It increases the losses, developed due to switching which reduces the capability of equipment (2) due to these harmonics ripples are generated in torque and speed of the motor (3) and it degrades the quality as well as the life of framework due to mechanical exhaustion and torque vibrations. When it is connected to an electrical network, the low harmonics are critically undesirable as they cause different issues at the distribution systems. To over-power these issues, enormous research had been done to control/reduce the impacts of harmonics in multilevel inverters. Proposing a proper switching plan for the power switches, which can generate the least Total Harmonic Distortion (THD), is the most vital perspective. In this paper, an improved optimization technique to decrease the harmonics is proposed, which efficiently decreases harmonics with less arithmetic computation. The productiveness of the proposed technique is also confirmed via simulations results and hardware setup.

Keywords- PWM, THD, Multilevel Inverter, Optimization, Trapezoidal Rule.

I. INTRODUCTION

Direct current (DC) is changed into alternating current (AC) by an inverter. In a perfect world voltage given by the inverters should be pure sinusoidal because it produces less noise and it is efficient in high voltage equipment [1]. But traditional three-level inverters can never acquire sinusoidal because of its low number of levels; subsequently, this produces more noise [2]. To handle this issue of a traditional inverter, multilevel inverters were presented. These inverters became much popular during recent years and they are commonly used for high voltage applications [3, 4]. The reason behind this efficiency of multilevel inverts is to provide a sinusoidal waveform which has less THD, lower electromagnetic hindrance and lesser work burden on switching devices. These subsequently increases the productivity and quality of voltage output provided by the inverter. Due to an increased number of samples in output voltage, a more sine-like waveform is generated which reduces THD in voltage output [5]. Regardless of this, the presence of unwanted harmonics in voltage output is a critical concern of inverters with multiple levels.

Cascaded multilevel inverters are popular and have various electric applications with lesser unwanted harmonics [6, 7]. Moreover, these inverters incorporate a medium rated voltage with low rated voltage using a specific arrangement of components. This specific property empowers it to achieve higher voltages with increased accessibility due to the redundancy of components in it. These features make this a better alternative for voltage inverters with medium range. On the other side, when these inverters are used for mechanical drives, the THD on the inverter output is not satisfactory owing to the fact that the operation of these drives is totally dependent on the nature of input voltage provided. Also, the low range harmonics are very undesirable in electrical grids as they create different problems for distribution network [8]. So the true objective is to control lower harmonics generated by multilevel inverters. There exist a couple of techniques to eliminate harmonics in the literature. These are commonly known as: sinusoidal Pulse Width Modulation (PWM) [9-12], Selective Harmonic Elimination and Space Vector Modulation (SVM) [13-14]. Still, these PWM methods also cannot diminish lower order harmonics perfectly.

In this paper, an improved PWM technique is presented which decreases the harmonic distortion further and it will, in general, have more efficient voltage level and angle calculations. These voltage levels and angles are then utilized for switching of inverters to reduce the Total Harmonic Distortion (THD). A most recent topology of inverter having exceedingly less number of switches is utilized for the execution of proposed technique to confirm its productiveness.

In order to show that the THD is reduced, simulations are done using SIMULINK in MATLAB along with hardware setup and then the comparative analysis is done using the Fourier Spectrum of output-voltage.
Paper outlines are as follows; Brief literature review is given in section II. The proposed optimization technique which minimized the THD is mentioned in Section III. Simulation results and analysis along with hardware setup are presented in section IV and section V respectively. Finally, the conclusion is made in section VI.

II. Literature Review

Total harmonic distortion is most essential because it occurs in a large number of inverters. Moreover, it is smaller in multilevel inverter than in any traditional inverter because of its expanded comparability with the sine-wave [15]. A couple of analysts have concentrated on generating a fruitful technique for further reduction of THD, thus different techniques have been presented in the research. Among these techniques, PWM got much attention due to its efficiency and compatibility with higher frequencies. However, these PWM techniques cannot reduce lower harmonics perfectly. SHE (Specific Harmonic Elimination) turns out to be a better substitute for targeted lower harmonics elimination using selective angles [16].
A straightforward method to manage SHE issue is the resultant theory method, where problematic linear equations of SHE are changed to practically identical polynomials. Furthermore, the resultant theory method is utilized to achieve each possible solution. In the event; if the amount of total harmonics increases, the degree of polynomial subsequently increases and at times it ends up being so huge that the solution of such equations does not exist. Therefore, mutative algorithms were used for solving such equations. The solution comes out from these algorithms disposes of lower range harmonics productively. These algorithms can be utilized for multilevel inverters without using any derivations. The enhanced calculations for multilevel inverters are presented in the literature as particle swarm optimization [17-19], bacterial search algorithm [20-21], bee algorithm [22] and genetic-algorithm [23-24].
The proper execution of such algorithms needs ideal decisions for certain parameters, for instance, transfer rate, size, initial guess, etc. Similarly, as cosine and sine elements of different frequencies are present in these equations, the convergence of these equations can be troublesome. This is a critical issue because the number of angles to be calculated increases with the number of levels of inverters. Additionally, solutions for the trigonometric equation are numerous, this creates more complexity for the decision of right angles. For instance, sometimes the determined angles do not have satisfactory distance from one another: the angle points turn out to be so close that it is nearly impractical to make a waveform derived from these edges. In this paper, an improved PWM technique is presented which decreases the further harmonic distortion and it will, in general, have more efficient voltage level and angle calculations. Moreover, this calculation procedure is independent of trigonometric terms consequently and reduces the computational burden and provides a solution without any convergence problem. The execution of this technique does not require any initial guess as well. To present the whole investigation a seven-level cascaded H-bridge is used but it is also shown that for any number of levels, switching angles alongside their voltages can be determined with this technique. The results are also proved via hardware

III. Proposed Technique

The proposed optimization technique will minimize the THD utilizing voltage levels and switching angles of the square wave calculated via equal-area estimation. The computational process will be free from trigonometric terms consequently less complex.
The steps to follow for the computational process are given below.

1. Selection of a reference sine-wave.
2. Its comparison with the output of the multi-level inverter.
3. Total area under the curve is distributed into trapezoids.
4. The voltage at various angles using this area are calculated.
5. To reduce the area, angles are modified accordingly.
6. Voltages are re-calculated using these modified angles.
7. Voltages levels are adjusted using input voltage sources of inverter accordingly.

Trapezoidal area of each trapezoid is calculated using eq (1), where Δx is the height and y is the base

$$\text{Area} = \Delta x\left(\frac{y_0}{2} + y_1 + y_2 + y_3 + \cdots + \frac{y_n}{2}\right) \qquad (1)$$

$$\text{Area} = \frac{\Delta x}{2}\,(y_0 + y_1) \qquad (2)$$

For this case, it can be used as eq (3)

$$\text{Area} = \frac{\Delta\theta}{2}\,(V_{\text{Previous}} + V_{\text{Next}}) \qquad (3)$$

Voltages present in trapezoidal rule (y_1,y_2) are calculated using eq (4)

$$V = V_m \text{Sin}\,\theta \qquad (4)$$

It can be modified for the given specific case as eq (5)

$$V_{\text{Instantaneous}} = V_{\text{Peak}} \text{Sin}\,\theta \qquad (5)$$

In the same way, voltage levels for a square wave are calculated using eq (3) and (4)

$$\text{Area} = V * \Delta\theta \tag{6}$$

For the specific case, it can be written as eq (7)

$$V_{\text{Square-wave}} = \frac{\text{Area Previously Calculated}}{\Delta\theta} \tag{7}$$

A comparison of the sine-wave with a square waveform of inverter output is done for the calculation of voltage levels and switching angles. Such comparison is shown in Fig-1 where an ideal sinewave is superimposed on square-wave which is the output of seven-level inverter.

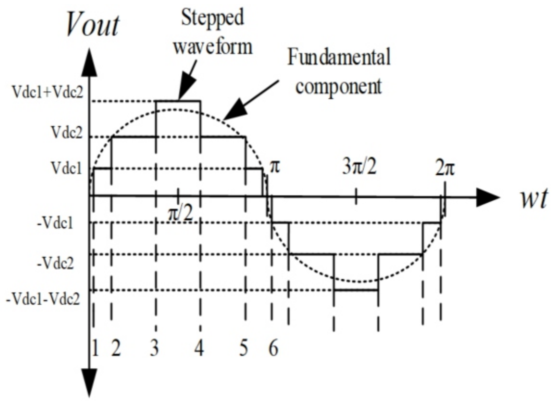

Fig. 1. Sine-wave superimposed on the output of the square wave for calculation

A perfect sine-wave having 40 V amplitude is compared with a square wave with the seven levels. The waveform of seven-level inverter to be compared is shown in Fig-2.

Fig. 2. Seven level square-wave used for comparison purpose

After the selection of an ideal sine wave, angles and respective voltages at each peak are calculated utilizing the number of levels involved and equations. Each area of the region represented by the numbers is calculated, if and only if it is a trapezoid. There emerges an issue because of trapezoidal rule, when the region from point 0 toward 1 and from 6 toward 7 ought to be zero as it is an ideal case, however from Fig-2, it is clear that it does not appear to be zero and there are some voltages over there. The area corresponding to the calculated voltage of 7-levels for typical PWM is shown in Table-1. The calculation in Table-1, consequently proves that the area represented as 1 and 7 creates a problem and produces 8.6774V, which is an ideal case and it should be zero.

To overcome this problem and to increase the effectiveness of the technique, areas under these segments are reduced by reducing the triggering angle of the first peak (keeping the voltage less than 1). The remaining amount of area from these sections are added into the peak interval of the square wave. Moreover, the remaining areas are decreased but keeping the symmetry of the signal. Table-2 verifies the effectiveness of modifications.

Moreover, in order to get better results and overcome this problem, these areas are reduced by reducing the triggering angle of the first peak (keeping the voltage less than 1). The remaining areas from this section is added to the peak interval of the square wave. Furthermore, the areas are decreased under the first curve by keeping the symmetry of the signal. Now for area 1 and 7, the calculated area and voltage are reduced to 1.368 and 0.691 as compared to the typical technique where the calculated area and voltages are 223.1332 and 8.6774 respectively. Similarly, the larger area of the typical technique is increased to 2350.313 from 1002.7688.

For each angle, area and voltages are calculated, then these values are used in a reduced switch inverter via the selection of suitable input voltages.

IV. Simulation and Results Analysis

To verify the effectiveness of the purposed technique, MATLAB simulations are used. Also for the sake of comparison inverter, two simulations are done; one is with the purposed technique, other is without. Moreover, tables and graphs are also presented to visualize the difference.

Fig-3 shows the circuit arrangement for this proposed technique, where a signal generator is connected to each of the switches in the circuit. The purpose of this signal generator is to provide the gate signal to the switches to generate the required output. This signal generator generates the PWM for each switch exactly at the same angels as calculated. The load is connected to voltmeter which is then connected to the THD block. The THD block calculates the THD of the signal and then the display block displays it.

Table 1. Switching Voltages corresponding to Calculated Areas for Typical Technique

Segment (n)	Angle $(\Delta\theta) = (180^o/7) * n$	Voltage (ΔV) = $40 * sin\,(\Delta\theta)$	Area = $0.5 * \Delta V * \Delta\theta$	Voltage = $Area\,/\,\Delta\theta$
1	25.714°	17.355	223.1332	8.6774
2	51.428°	31.273	625.2101	24.3139
3	77.142°	38.997	903.4613	35.1349
4	102.856°	38.997	1002.7688	38.9969
5	128.57°	31.273	903.4613	35.1349
6	154.284°	17.356	625.2101	24.3144
7	180°	0	223.1332	8.6779

Table 2. Switching Voltages corresponding to Calculated Areas for Proposed Technique

Segment (n)	Calculated Angles $(\Delta\theta)$	Voltage (ΔV) = $40 * sin\,(\Delta\theta)$	Calculated Area = $0.5 * \Delta V * \Delta\theta$	Calculated Voltage = Calculated $Area\,/\,\Delta\theta$
1	1.98°	1.3820	1.368	0.691
2	27.694°	18.59	256.754	9.985
3	53.408°	32.116	651.927	25.353
4	126.59°	49.448	2350.313	32.116
5	152.306°	18.59	651.927	25.353
6	178.02°	1.3820	256.754	9.985
7	180°	0	1.368	0.691

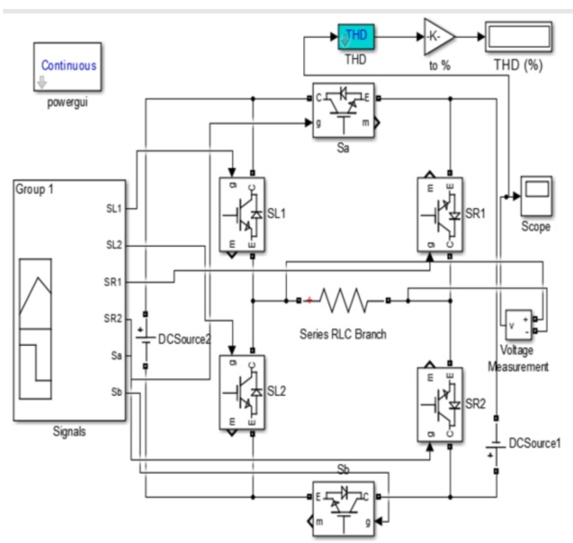

Fig. 3. The circuit arrangement of inverter in MATLAB

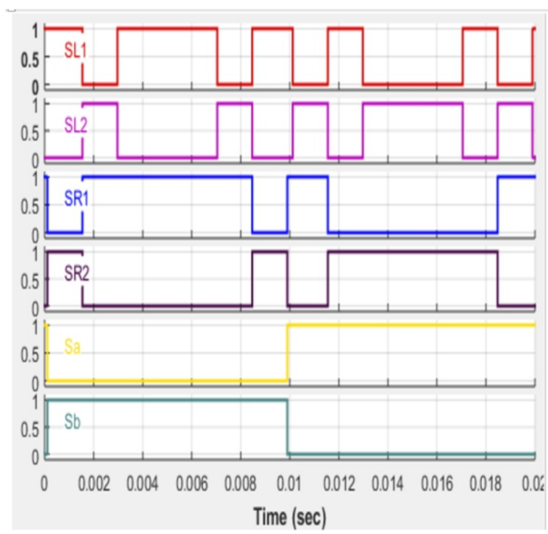

Fig. 4. Proposed PWM for multilevel inverter

The PWM waveform according to the proposed solution is shown in Fig-4. This is the switching ON and OFF pattern of all the switches respectively. *SL1* and *SL2* have exactly the opposite PWM than each other, while *S*R1, SR1, and *Sa*, *Sb* have also the same scenarios.

The trigger ON and OFF values of these signals are presented in Table-3 i.e. the start and end time for the first interval of *SL1, SR1* and *Sa* will be *0* to *0.11m - sec* and so on. It is clear when the voltage is rising from zero volts, the interval is short for each switch there and after that. Moreover, each interval is equally distributed except for the peak voltage interval.

Table 3. Switching angles duty cycle for Proposed PWM

Voltage Level	Time Required ($m-sec$)	ON Switches
0	0	$SL1, SR1, Sa$
V	0.11	$SL1, SR2, Sb$
$3V$	1.54	$SL2, SR1, Sb$
$4V$	2.97	$SL1, SR1, Sb$
$3V$	7.04	$SL2, SR1, Sb$
V	8.47	$SL1, SR2, Sb$
0	9.9	$SL1, SR1, Sa$
0	10.01	$SL1, SR1, Sa$
$-V$	10.12	$SL2, SR1, Sa$
$-3V$	11.55	$SL1, SR2, Sa$
$-4V$	12.98	$SL2, SR2, Sa$
$-3V$	17.05	$SL1, SR2, Sa$
$-V$	18.48	$SL2, SR1, Sa$
0	0.0199	$SL1, SR1, Sa$
0	0.02	$SL1, SR1, Sa$

Fig-5 presents the THD of the resultant waveform when a typical PWM technique is used for the multilevel inverter. With typical PWM, the first and second harmonics appear to be large enough which in turn increases the THD, which comes out to be 31.05%.

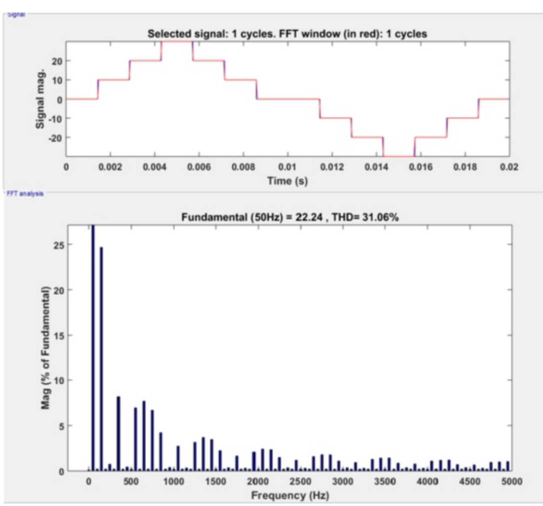

Fig. 5. Total Harmonic Distortion of output waveform with typical PWM

Fig-6 contains waveform with calculated THD when proposed PWM technique is used. It is clear from the figure that first and second harmonics are considerably reduced due to which THD has dramatically decreased and appears to be 13.13% which is best suited for domestic use of this inverter according to the IEEE standard. This confirms the effectiveness of this proposed improved PWM technique.

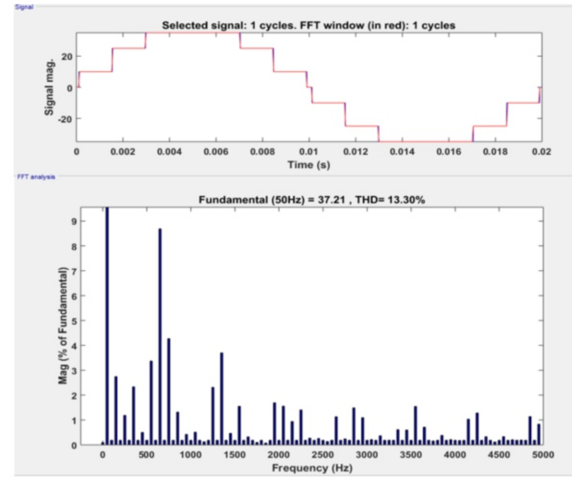

Fig. 6. Total Harmonic Distortion of output waveform with Proposed PWM

V. HARDWARE IMPLEMENTATION

A single-phase 7-level inverter has been assembled utilizing two diverse DC sources, driver's circuit and IGBTs as the switching devices. A different power supply for driver hardware of *12V* is developed utilizing step-down transformers along with rectifier circuitry is additionally used. Atmega 89C52 microprocessor with *2MHz* clock and an I/O card is used to generate pulses. Moreover, pulses are given to the switching devices through a delay circuitry to keep it safe from the short circuit because of concurrent conduction of similar leg of H-bridge. In addition, DC source appended with switching circuitry has got the same values as calculated in Section 3, which is *9v* and *26v.* The hardware setup of the complete model is shown in Fig-7.

Fig. 7. Hardware Setup of 1-Phase 7-Level Inverter

To validate the theoretical and simulation results, this model using the same pulses as mentioned in Table-3.

The phase voltage and its experimental THD are shown in Fig-8. The THD spectrum demonstrates that first and second harmonics are lessened as anticipated analytically. Furthermore, the THD as processed theoretically and experimentally are 13.30% and 13.56% respectively. The above information demonstrates that test results are in close concurrence with the hypothesis.

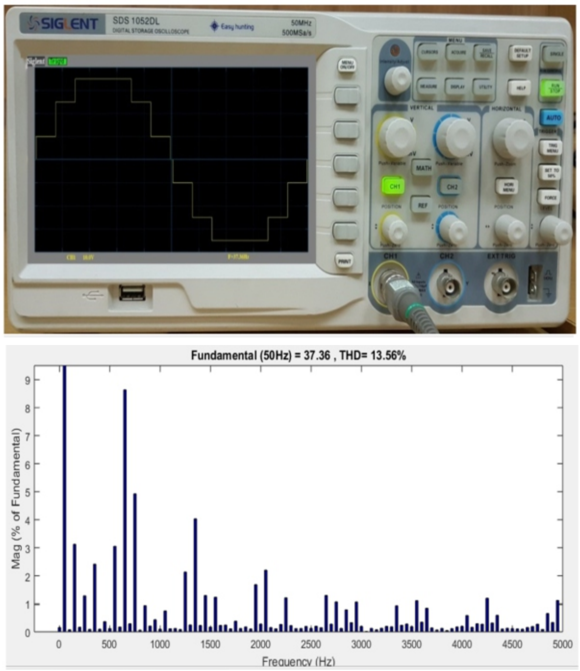

Fig. 8. Output Voltage and THD using experimental Setup

VI. Conclusion

The recent control pattern for multilevel-inverters has a higher quality of power which results in higher efficiency. Therefore traditional PWM techniques for control such as space-vector PWM does not turn out to be finest methodologies due to their higher switching frequencies. The SHE system has ascended as a capable control procedure for multilevel-inverters. Regardless, the inconvenience for the SHE system is to resolve complex harmonic equations and for the entire modulation-index its solution is not valid. That is the reason it does not completely clear out all of the harmonics present in the system to satisfy the application necessities.

To resolve this issue an improved technique dependent on equal area PWM is proposed which turns out to be the finest and less unpredictable than SHE. The efficiency of proposed technique is confirmed by MATLAB simulations and hardware setup implemented on reduced switch topology of the multilevel inverter.

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